

REALIZATION OF 1=2 TERNARY LOGIC GATES (BUILDING BLOCK) USING MOSFET

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ABSTRACT

In this paper, we discuss the practical realization of 1=2 Logic gates using MOSFET. The 1=2 logic gate design is a hitherto unimplemented and unused design. Current circuitry based on the logic of aforementioned gates is complex since it uses registers and counters. The present CMOS technology does not use depletion mode transistors. The prime objective in our work is to minimize the number of transistors used, eliminate the use of resistors to lower the power consumption, reduce the propagation delay time and eliminate depletion mode transistors. The reduction in the number of transistors is main focus as that enabled a more compact design which utilized the less chip area.

KEYWORDS: 1=2 Logic Gates, Basic Gates, Integrated Circuit, MOSFET, Multi-Valued Logic Design, Ternary Logic